## 1503240112

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# DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/MANAGEMENT/ COMMERCIAL PRACTICE, APRIL - 2025

# **DIGITAL CIRCUITS**

[Maximum marks: 100]

[Time: 3 Hours]

 $(5 \ge 2 = 10)$ 

 $(5 \times 6 = 30)$ 

# PART – A

#### Maximum marks: 10

I. (Answer *all* the questions in one or two sentences. Each question carries 2 marks)

- 1. Define Radix of a number system.
- 2. Write Identity rule of Boolean expression.
- 3. Write the truth table of a NOR gate.
- 4. Define Shift register.
- 5. Define the term Capacity of a Memory.

## PART – B

#### Maximum marks: 30

- **II.** (Answer any *five* of the following questions. Each question carries 6 marks)
  - 1. Convert (i)  $(572)_8 = (\dots)_{16}$  (ii)  $(34F)_{16} = (\dots)_{10}$  (iii)  $(72.3125)_{10} = (\dots)_2$
  - 2. Implement AND, OR and NOT gates using NAND gates.
  - 3. With diagram explain the operation of 4 to 1 Multiplexer.
  - 4. Explain the working of D Latch.
  - 5. Describe the working principle of 4-bit Synchronous counter.
  - 6. Explain the operation of binary weighted resistor type DAC.
  - 7. Explain the specifications of digital meter display.

## PART – C

#### Maximum marks: 60

(Answer one full question from each unit. Each full question carries 15 marks)

## UNIT – I

**III**. (a) Solve the following (i) 11011-10110 (using 2's complement method)

(ii) 1100 - 1001 (iii)  $101111 \div 101$  (iv) 1110x101 (8)

(b) Simplify the Logic expression AB + A(B+C)+B(B+C) (7)

# OR

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(a) Simplify the Boolean Function $F(A, B, C, D) = \sum m (1,3,7,11,15) + \sum d (0,2,5)$	(8)
(b) Compare weighted and Un weighted code.	(7)
UNIT - II	
(a) With diagram explain the operation of a Parallel Binary Adder.	(8)
(b) With neat diagram explain the operation of TTL NOT gate.	(7)
OR	
(a) Describe the operation of 2-bit Comparator.	(8)
(b) Describe the operation of 1x4 De-Multiplexer.	(7)
UNIT - III	
(a) Explain the operation of JK Flip Flop.	(7)
(b) Describe the operation of asynchronous UP counter.	(8)
OR	
(a) Explain the operation of Serial-in-Serial-out Shift Register.	(7)
(b) Explain D Flip Flop with help of truth table.	(8)
UNIT – IV	
(a) Explain the operation of Successive approximation A/D Convertor.	(8)
(b) Compare RAM and ROM.	(7)
OR	
(a) Describe about various types of ROM.	(7)
(b) Explain the operation of R-2R D/A converter.	(8)
	<ul> <li>(b) Compare weighted and Un weighted code.</li> <li>UNIT - II</li> <li>(a) With diagram explain the operation of a Parallel Binary Adder.</li> <li>(b) With neat diagram explain the operation of TTL NOT gate.</li> <li>OR</li> <li>(a) Describe the operation of 2-bit Comparator.</li> <li>(b) Describe the operation of 1x4 De-Multiplexer.</li> <li>UNIT - III</li> <li>(a) Explain the operation of JK Flip Flop.</li> <li>(b) Describe the operation of asynchronous UP counter.</li> <li>OR</li> <li>(a) Explain the operation of Serial-in-Serial-out Shift Register.</li> <li>(b) Explain D Flip Flop with help of truth table.</li> <li>UNIT - IV</li> <li>(a) Explain the operation of Successive approximation A/D Convertor.</li> <li>(b) Compare RAM and ROM.</li> <li>(a) Describe about various types of ROM.</li> </ul>

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