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N22 – 07887

Reg. No……
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DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/ MANAGEMENT/COMMERCIAL PRACTICE, NOVEMBER – 2022

DIGITAL ELECTRONICS

[Maximum Marks: **100**] [Time: **3** Hours]

PART-A

[Maximum Marks: **10**]

I. (Answer ***all*** questions in one or two sentences. Each question carries ***2*** marks)

1. Name the Unweighted code in which the successive codes differs by only one bit.
2. State De-Morgan's theorem.
3. Define the term Fan-out.
4. Identify the need for Master Slave JK flip flops.
5. Calculate the number of flip flops required to construct a Mod-30 counter. (5 x 2 = 10)

PART-B

[Maximum Marks: **30**]

II. (Answer ***any five*** of the following questions. Each question carries ***6*** marks)

1. Convert the following.

   (a) $(726)_{10}=(X)_2$ (b) $(101011011)_2=(X)_{16}$ (c) $(1C7)_{16}=(X)_{10}$

2. "NAND gate is a universal gate" Justify this by designing a NOR gate using NAND gates only.
3. Draw and explain the circuit of TTL inverter.
4. Write the working of a Full adder circuit with truth table.
5. Identify any three differences between synchronous and asynchronous sequential logic circuits.
6. Draw and explain the working of a SR flip flop using NAND gates.
7. Draw and describe the working of a counter which count from 0 to 7 with synchronous input.

(5 x 6 = 30)

PART-C

[Maximum Marks: **60**]

(Answer ***one*** full question from each Unit. Each full question carries **15** marks)

UNIT – I

III. (a) Minimise the following function using K Map, and realize using logic gates.

$F=\Sigma_m(0,2,3,4,6,7,10,11,12,14,15)$ (10)

(b) Subtract 1001 from 1111 by using 2's complement method. (5)

OR

IV. (a) Design a circuit for the following function through SOP form.

$F=_{(ABC)}=\Sigma_m(0,2,3,4,6,7)$ (9)

(b) Write short note on the need for binary number system in digital technology. (6)

UNIT – II

V. (a) With a block diagram, explain the working of a 4 bit parallel binary adder. (9)

(b) Compare SSI,MSI, LSI and VLSI levels of integration. (6)

OR

VI. (a) Explain the operation of a 4 X 1multiplexer with block diagram, truth table and expression. (9)

(b) Compare TTL with CMOS logic family in terms of any three parameters. (6)

UNIT- III

VII. (a) With necessary diagrams explain the working of SISO, SIPO, PIPO, and PISO shift registers. (12)

(b) Construct a D flip flop using SR flipflop and draw its truth table. (3)

OR

VIII. (a) Draw and explain the operation of a Ring Counter. (8)

(b) Draw the block diagram and explain the operation of a Master Slave JK flip flop. (7)

UNIT - IV

IX. (a) Draw and explain the operation of a Successive Approximation type ADC. (9)

(b) Define the following terms of a DAC.

(i) Resolution (ii) Accuracy (iii) Settling time (6)

OR

X. (a) With a neat diagram explain the operation of a 3 bit Up-Down counter. (8)

(b) Illustrate the working of a R-2R ladder type DAC. (7)

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