

THIRD SEMESTER DIPLOMA EXAMINATION IN
ENGINEERING/TECHNOLOGY — OCTOBER, 2016

DIGITAL COMPUTER PRINCIPLES
(Common for CT and CM)

[Time : 3 hours

(Maximum marks : 100)

PART — A

(Maximum marks : 10)

Marks

I Answer the following questions in one or two sentences. Each question carries 2 marks.

1. State the base of a number system.
2. One's compliment of 1011 is
3. Reduce the expression $f(A, B, C) = \sum_m(0, 1, 2, 3, 4, 5, 6, 7)$.
4. Name the flipflop used for data storage.
5. Name an error detecting code.

(5×2 = 10)

PART — B

(Maximum marks : 30)

II Answer any five questions from the following. Each question carries 6 marks.

1. Convert 1011 to gray code and gray code 1100 to binary.
2. Map the expression $f = A'B'C + AB'C + A'BC' + ABC' + ABC$.
3. Demonstrate a one bit comparator.
4. Compare sequential and combinational circuit.
5. Draw a 4 bit ring counter using D Flipflop.
6. State the DAC Parameters - Accuracy and Settling time.
7. Draw an internal logic diagram of 32×8 ROM.

(5×6 = 30)

PART — C

(Maximum marks : 60)

(Answer *one* full question from each unit. Each full question carries 15 marks.)

UNIT — I

- III (a) Convert the following :
- (i) $(237.25)_{16}$ to Octal
 - (ii) $(11010011.1111)_2$ to Hexadecimal
 - (iii) 232.17 to Binary 9
- (b) Expand $A' + B'$ to min terms and max terms. 6

OR

- IV Describe any 7 laws of Boolean Algebra. 15

UNIT — II

- V (a) Design a full adder. 9
- (b) Reduce the expression $f = \sum m(0, 2, 3, 4, 5, 6)$ using K-map. 6

OR

- VI Demonstrate a 4 bit adder-subtractor with suitable neat diagram. 15

UNIT — III

- VII (a) Demonstrate a JK Flipflop with Truth Table. 9
- (b) Construct a T Flipflop using a JK Flipflop with Truth Table 6

OR

- VIII Demonstrate a 4 bit parallel in serial out shift register. 15

UNIT — IV

- IX Explain a weighted resistor type DAC. 15

OR

- X Draw a logic diagram to implement the Boolean functions.
- $F1 = AB' + AC + A'BC'$
- $F2 = (AC + BC)'$ in PLA with a PLA programming table. 15