TED (15) – 3131

(REVISION — 2015)

Reg. No.....

Signature .....

DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/ MANAGEMENT/COMMERCIAL PRACTICE — APRIL, 2018

COMPUTER ARCHITECTURE (CT)

[*Time* : 3 hours

(Maximum marks : 100)

PART — A

(Maximum marks : 10)

Marks

I Answer *all* questions in one or two sentences. Each question carries 2 marks.

1. Mention any two examples for program Interrupts.
2. Define Programmed I/O.
3. Define seek time.
4. Define PSW.
5. Define microprogram. (5×2 = 10)

PART — B

(Maximum marks : 30)

II Answer any *five* of the following questions. Each question carries 6 marks.

1. Draw and explain Von-Neuman architecture.
2. Draw the timing diagram of synchronous bus operation.
3. How the data are written into a magnetic disk.
4. Explain any four DMA functions.
5. Draw the typical format of horizontal and vertical microinstructions.
6. Explain different types of data hazards.
7. List and explain different types of ROM. (5×6 = 30)

Marks

PART — C

(Maximum marks : 60)

(Answer *one* full question from each unit. Each full question carries 15 marks.)

UNIT — I

III (a) List the different types of transfers the interconnection structures should support. 5

(b) Explain briefly the elements of bus design. 10

OR

IV Briefly explain the elements of cache design. 15

UNIT — II

V (a) Explain the steps of interrupt processing. 7

(b) List the design issues arise in implementing interrupt driven I/O. Mention and explain the different techniques used for handling the design issues. 8

OR

VI (a) Consider a magnetic disk drive with 16 surfaces, 512 tracks per surface and 64 sectors per track. The sector size is 1KB. The average seek time is 6ms, the track to track access time is 1 ms and the drive rotates at 3600 rpm. Successive tracks in a cylinder can be read without head movement. Then

(i) What is the disk capacity ? 4

(ii) Calculate the average access time. 8

(b) Define the terms rotational delay, access time and transfer time. 3

UNIT — III

VII (a) Draw and explain the instruction cycle state diagram. 10

(b) Explain the common flags in PSW. 5

OR

VIII (a) Assume a pipeline with four stages such as Fetch Instruction (IF), Decode instruction and calculate address(DA), Calculate Operans(CA), Fetch operand (FO), Execute(EX) and Write Operands(WO). Draw a diagram for a sequence of 15 instruction and assume that instruction 3 is a conditional branch to instruction 15 and in which there are no data dependencies. 10

(b) What general roles are performed by processor register ? 5

UNIT — IV

IX (a) Draw and explain the hardwired implementation. 8

(b) Draw and explain the block diagram of control unit. 7

OR

X (a) List and explain Flynn's classification of parallel processing system. 9

(b) Explain symbolically the different sequence of events occur during Fetch and Interrupt cycle. 6

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